REMARKS

This Request for Reconsideration is filed in response to the Office Action of November 16, 2006 in which claims 1-22 were rejected.

Claims 1-22 are rejected under 35 U.S.C. Section 103(a) as being unpatentably obvious over *Ootani et al* (US 6,959,365), in view of *Kanehira et al* (US 2003/0110361).

Ootani et al show a flash memory module 2 that outputs a ready status signal (RYIBY) indicating whether a rewrite operation is being executed as commanded by a CPU 1. It sends this ready status signal to a flash memory circuit 3 which in turn sends a HOLD signal (see Fig. 1) to the CPU 1 in order to indicate to the CPU that access to the flash memory portion should be fixed to a constant value. As admitted by the Examiner, *Ootani et al* do not teach performing detection of processing errors and changing the status of the ready/busy line back to the busy status if a processing error is detected.

The Examiner, however, points to *Kanehira et al* for teaching performing detection of processing errors and changing the status of said ready/busy line back to said busy status if a processing error is detected, pointing to section [0064], lines 28-43.

Kanehira et al has been carefully reviewed and the Examiner's conclusion about the ready/busy line is incorrect. The only thing shown about the ready/busy line in any of the examples of *Kanehira et al* is for a confirmation of write completion. It does not have anything to do with changing to a busy status if a processing error is detected.

Kanehira et al is concerned with error handling, but it is of a different character than that addressed by the present invention. *Kanehira et al* is concerned with a real-time application of a flash memory system such as the camera

application shown in Fig. 3. In such an application, the signal processing capabilities may be fairly limited and may be unable to conduct error correction rewriting operations of fast-moving image frames without breaking down. See the last sentence of paragraph [0004] and the last sentence of [0009] on the same page. The way *Kanehira et al* avoid this problem is basically by not bothering to rewrite frames that are subject to error and just skipping the whole process because it probably will not be noticed anyway. The way this is expressed by *Kanehira et al* is to say that, for example, "the rewriting of next data is instructed with respect to the write error produced in the data area without instructing the rewriting of the same data to thereby assure a write speed of a predetermined rate or more, whereby an effective record rate is avoided from falling below a rate for write data." See the first sentence of paragraph of [0009] on page 1 or paragraph [0010] where it is stated "...the memory control unit may be configured so as to transmit error information to the memory controller without rewriting when an error occurs upon the writing to the memory unit." This is repeated many times throughout the *Kanehira et al* specification.

In the *Kanehira et al* specification, the ready/busy signal is merely used for notifying to the outside of the chip whether the memory chip 16 is in a ready state or a busy state (see the last sentence of paragraph [0041] on page 3).

The skipping of the rewriting to the data area 13 is best shown in Fig. 7 at reference numeral 71 as described at page 5, paragraph [0055] where it is stated that "...the writing is completed without making the error discrimination based on the Status information upon the writing to the data area 13 (71). Namely, neither of rewriting (52) by the memory control unit 14 nor transmission (53) of error information from the memory control unit 14 to the flash memory controller 15 is done. This is done to omit such a process as to give priority to a real-time property of the data written into the data area 13 and inhibit the real-time property thereof as far as practicable."

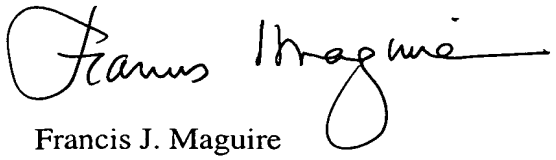
Again, the above-mentioned inhibition of a real-time property of the data is omitted and therefore this becomes effective in avoiding a failure in the system due to the fact that the effective record rate falls below the rate for the right data (see the last sentence of paragraph [0058]). This is somewhat convoluted way of saying it but the meaning is that they don't rewrite the data even though there is an error. And, a careful study of the entire reference will make it clear that there is no use of the ready/busy signal or any other of the signals shown between the flash memory and the flash memory controller in the way claimed in the present invention, i.e., to change the status of the line back to the busy status if a processing error is detected.

The *Ootani et al* reference has also been studied carefully and there is nothing like the present invention shown there either.

Therefore, both the *Ootani et al* and the *Kanehira et al* references are inapplicable as 35 U.S.C. Section 103(a) references against claims 1-22 and withdrawal of the obvious rejection thereof on that ground is requested.

The objections of the Office Action of November 16, 2006, having been obviated by amendment or shown to be inapplicable, withdrawal thereof is requested and passage of claims 1-22 to issue is earnestly solicited.

Respectfully submitted,



Francis J. Maguire
Attorney for the Applicant
Registration No. 31,391

FJM/lk
WARE, FRESSOLA, VAN DER SLUYS
& ADOLPHSON LLP
755 Main Street, P.O. Box 224
Monroe, Connecticut 06468
(203) 261-1234